Claims

I claim:

1. A vacuum packaged array of electromechanical micromirror devices comprising:

a device substrate having a 1st surface and a 2nd surface;

control circuitry disposed on said 1st surface of said device substrate;

an array of micromirror sections disposed on said 2nd surface of said device substrate, wherein each said micromirror section comprises:

a micromirror;

at least 1 support structure for supporting said micromirror; and

at least 1 addressing electrode for actuating said micromirror;

a plurality of electrically conductive routing lines integral with said device substrate that connects said control circuitry to said at least 1 addressing electrode;

a 1st plurality of metallic terminals disposed on said 1st surface of said device substrate that are electrically connected with said control circuitry;

a 1st packaging substrate having a 1st surface and a 2nd surface;

a 2nd plurality of metallic terminals disposed on said 1st surface of said 1st packaging substrate;

a plurality of solder balls electrically connecting said 1st plurality of metallic terminals to said 2nd plurality of metallic terminals and thereby mounting said device substrate on said 1st packaging substrate;

a 2nd packaging substrate being adhered to said 1st surface of said 1st packaging substrate by a glass frit bonding line that surrounds said device substrate; and

an evacuated region bounded by said packaging substrates and said glass frit bonding line.

2. The vacuum packaged array of claim 1, wherein said control circuitry is selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistors circuits.

3. The vacuum packaged array of claim 1, wherein said device substrate is selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP.

4. The vacuum packaged array of claim 1, wherein said electrically conductive routing lines between said control circuitry and said at least 1 addressing electrode comprises at least 1 via through said device substrate and a metallization in said at least 1 via.

5. The vacuum packaged array of claim 1, wherein said device substrate additionally comprises an insulating layer between said 1st surface and said 2nd surface.

6. The vacuum packaged array of claim 1, wherein said micromirror is a metallic mirror.

7. The vacuum packaged array of claim 1, wherein said micromirror is a multilayer dielectric mirror.

8. The device of claim 1, wherein the reflective side of said micromirror is substantially planar with neither recesses nor protrusions.

9. The vacuum packaged array of claim 1, wherein said micromirror has no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate.

10. The vacuum packaged array of claim 9, wherein said micromirror is in the shape of a polygon.

11. The vacuum packaged array of claim 10, wherein said polygon is selected from the group consisting of a rectangle and a hexagon.

12. The vacuum packaged array of claim 1, wherein said micromirror section additionally comprises:

a torsion hinge that is disposed to support said micromirror support structure; and

a pair of support structures for said torsion hinge that supports said torsion hinge on said substrate.

13. The vacuum packaged array of claim 1, wherein said micromirror section additionally comprises at least 1 stopping member that limits the rotation of said micromirror.

14. The vacuum packaged array of claim 13, wherein said at least 1 stopping member comprises:

a 1st stopping member that limits the rotation of said micromirror in a 1st direction; and

a 2nd stopping member that limits the rotation of said micromirror in a direction opposite to said 1st direction.

15. The vacuum packaged array of claim 1, wherein said 1st packaging substrate is electrically insulating.

16. The vacuum packaged array of claim 15, wherein said 1st packaging substrate is selected from the group consisting of ceramic, glass, quartz, sapphire, plastic, a semiconductor with a dielectric coating, and a metal with a dielectric coating.

17. The vacuum packaged array of claim 1, wherein said 2nd packaging substrate is transparent to electromagnetic radiation.

18. The vacuum packaged array of claim 17, wherein said 2nd packaging substrate is selected from the group consisting of glass, quartz, sapphire, plastic, and semiconductors.

19. The vacuum packaged array of claim 18, wherein said semiconductor is silicon.

20. The vacuum packaged array of claim 1, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit, a solvent, and a binder.

21. The vacuum packaged array of claim 1, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit with a glass transition temperature of less than 400 °C.

22. The vacuum packaged array of claim 21, wherein said glass frit has a glass transition temperature of less than 350 °C.

23. The vacuum packaged array of claim 22, wherein said glass frit has a glass transition temperature of less than 300 °C.

24. The vacuum packaged array of claim 1, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit with a softening temperature of less than 450 °C.

25. The vacuum packaged array of claim 24, wherein said glass frit has a softening temperature of less than 400 °C.

26. The vacuum packaged array of claim 25, wherein said glass frit has a softening temperature of less than 350 °C.

27. The vacuum packaged array of claim 1, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit that contains 45 to 90 % PbO by weight.

28. The vacuum packaged array of claim 1, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit and a particulate filler material, said particulate filler material having a melting point higher than that of said glass frit.

29. The vacuum packaged array of claim 1, wherein an evacuation tube is disposed between said packaging substrates.

30. The vacuum packaged array of claim 1, wherein an evacuation tube is sealed on an opening in said 2nd surface of said 1st packaging substrate.

31. The vacuum packaged array of claim 1, additionally comprising a getter material that is disposed in the interior of said evacuated region.

32. The vacuum packaged array of claim 31, wherein said evacuated region comprises a 1st portion and a 2nd portion and a non-sealing barrier therebetween, wherein

said 1st portion contains said device substrate;

said 2nd portion contains said getter material; and

said non-sealing barrier allows gas diffusion between said 1st portion and said 2nd portion.

33. The vacuum packaged array of claim 1, wherein said evacuated region has a pressure of less than approximately 1×10^{-4} torr (approximately 1.33×10^{-2} Pa).

34. The vacuum packaged array of claim 33, wherein said evacuated region has a pressure of less than approximately 1×10^{-6} torr (approximately 1.33×10^{-4} Pa).

35. A spatial light modulator (SLM) comprising a vacuum packaged array according to claim 1.

36. A method of fabricating a vacuum packaged array of electromechanical micromirror devices, comprising the steps of:

providing a device substrate with a 1st surface and a 2nd surface;

forming control circuitry on said 1st surface of said device substrate;

forming a plurality of micromirror sections on said 2nd surface of said device substrate, comprising the steps of;

forming a plurality of addressing electrodes for actuating micromirrors;

forming a plurality of support structures for supporting said micromirrors; and

forming a plurality of micromirrors such that they are supported by said support structures; and

forming a plurality of electrically conductive routing lines that are integral with said device substrate that connects said control circuitry to said at least 1 addressing electrode;

forming a 1st plurality of metallic terminals disposed on said 1st surface of said device substrate that are electrically connected with said control circuitry;

providing a 1st packaging substrate having a 1st surface and a 2nd surface;

forming a 2nd plurality of metallic terminals on said 1st surface of said 1st packaging substrate;

depositing a plurality of solder balls on either of said plurality of metallic terminals;

electrically connecting said 1st plurality of metallic terminals to said 2nd plurality of metallic terminals and thereby mounting said device substrate on said 1st packaging substrate;

providing a 2nd packaging substrate;

adhering said 2nd packaging substrate to said 1st surface of said 1st packaging substrate by sealing at a glass frit bonding line that surrounds said device substrate (package sealing step); and

forming an evacuated region bounded by said packaging substrates and said glass frit bonding line (evacuation step).

37. The method of claim 36, wherein said step of forming control circuitry comprises a step of fabricating circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

38. The method of claim 36, wherein said device substrate is selected from the group consisting of silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP.

39. The method of claim 36, wherein said step of forming electrically conductive routing lines that connect said control circuitry and said at least 1 addressing electrode comprises the steps of:

forming at least 1 via through said device substrate; and

forming a metallization in said at least 1 via.

40. The method of claim 36, wherein said device substrate additionally comprises an insulating layer disposed between said 1st surface and said 2nd surface.

41. The method of claim 36, wherein said step of forming a micromirror comprises a step of forming a reflective metallic coating.

42. The method of claim 36, wherein said step of forming a micromirror comprises a step of forming a reflective multilayer dielectric coating.

43. The method of claim 36, wherein said step of forming micromirror sections comprises the steps of:

forming said plurality of micromirror support structures such that it is embedded in a layer of sacrificial material;

planarizing said sacrificial layer such that said sacrificial layer and the top of said micromirror support structure are substantially planar;

depositing a micromirror material on said planar surface;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

44. The method of claim 36, wherein said sacrificial layer material is selected from the group consisting of photoresist polymer, silicon oxide, silicon nitride, silicon oxynitride, and amorphous silicon.

45. The method of claim 44, wherein said planarizing step comprises a chemical mechanical polishing (CMP) process.

46. The method of claim 36, wherein said step of forming a plurality of micromirrors comprises a step of:

patterning each micromirror such that its reflective surface has no edges that are perpendicular to the projection of the incident light propagation vector onto the plane of said device substrate.

47. The method of claim 36, wherein each said micromirror is patterned to be in the shape of a polygon.

48. The method of claim 47, wherein said polygon is selected from the group consisting of a rectangle and a hexagon.

49. The method of claim 36, additionally comprising a step of forming a torsion hinge for supporting each said micromirror support structure, said step comprising:

forming a plurality of support structures for supporting torsion hinges; and

forming a plurality of torsion hinges.

50. The method of claim 36, additionally comprising a step of:

forming at least 1 stopping member that limits the rotation of each said micromirror.

51. The method of claim 50, wherein said step of forming at least 1 stopping member comprises:

forming a 1st stopping member that limits the rotation of each said micromirror in a 1st direction; and

forming a 2nd stopping member that limits the rotation of each said micromirror in a direction opposite to said 1st direction.

52. The method of claim 36, wherein said 1st packaging substrate is electrically insulating.

53. The method of claim 52, wherein said 1st packaging substrate is selected from the group consisting of ceramic, glass, quartz, sapphire, plastic, a semiconductor with a dielectric coating, and a metal with a dielectric coating.

54. The method of claim 36, wherein said 2nd packaging substrate is transparent to electromagnetic radiation.

55. The method of claim 54, wherein said 2nd packaging substrate is selected from the group consisting of glass, quartz, sapphire, plastic, and semiconductors.

56. The method of claim 55, wherein said semiconductor is silicon.

57. The method of claim 36, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit, a solvent, and a binder.

58. The method of claim 36, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit with a glass transition temperature of less than 400 °C.

59. The method of claim 58, wherein said glass frit has a glass transition temperature of less than 350 °C.

60. The method of claim 59, wherein said glass frit has a glass transition temperature of less than 300 °C.

61. The method of claim 36, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit with a softening temperature of less than 450 °C.

62. The method of claim 61, wherein said glass frit has a softening temperature of less than 400 °C.

63. The method of claim 62, wherein said glass frit has a softening temperature of less than 350 °C.

64. The method of claim 36, wherein the glass frit composition that is used to form said glass frit bond line comprises a glass frit that contains 45 to 90 % PbO by weight.

65. The method of claim 36, wherein the glass frit composition that is used to form said glass frit bonding line comprises a glass frit and a particulate filler

material, said particulate filler material having a melting point higher than that of said glass frit.

66. The method of claim 36, additionally comprising the step of:

providing an evacuation tube;

positioning said evacuation tube such that a portion of said evacuation tube is located in the interior of the region bounded by said packaging substrates and glass frit bonding line;

adhering said packaging substrates at said glass frit bonding line;

evacuating said package through said evacuation tube after said package sealing step; and

sealing said evacuation tube.

67. The method of claim 36, additionally comprising the steps of:

providing an evacuation tube;

sealing said evacuation tube on an opening in said 2nd surface of said 1st packaging substrate;

evacuating said package through said evacuation tube after said package sealing step; and

sealing said evacuation tube.

68. The method of claim 36, additionally comprising the steps of:

providing a getter material;

positioning said getter material within the interior of the region bounded by said packaging substrates and glass frit bonding line before said package sealing step; and

activating said getter after said evacuation step.

69. The method of claim 36, additionally comprising the steps of:

providing a 1st region within the the interior of the region bounded by said packaging substrates and glass frit bonding line, said 1st region containing said device substrate;

providing a 2nd region within the the interior of the region bounded by said packaging substrates and glass frit bonding line;

providing a non-sealing barrier between said 1st region and said 2nd region;

providing a getter material;

positioning said getter material in said 2nd region before said package sealing step; and

activating said getter after said evacuation step.